КП7117А-5
(60N035)

N-Channel Field Effect Transistor

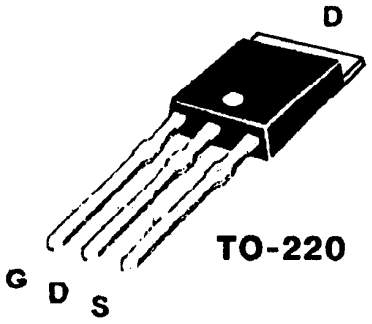
Preliminary June 2001

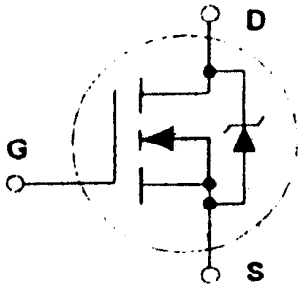
General Description

These n-channel power field effect transistors are produced using high cell density DMOS technology. These devices are particularly suited for low voltage applications such as automotive and other battery powered circuits where fast switching, low in-line power loss and resistance to transients are needed.

Features

- 60 A, 30 V, $R_{DS(ON)}$ = 0.015Ω
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppresser.
- Super high density cell design for extremely low $R_{DS(ON)}$.





Absolute Maximum Ratings (T_C = 25°C unless otherwise noted)

Symbol	Parameter	603	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current - Continuous - Pulsed	 60 180	A
P_D	Total Power Dissipation @ T_C = 25°C	50	W
	Derate above 25°C	0.4	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-65 to 175	°C

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V V_{GS} = 0 V			10	μA
I_{GSSF}	Gate-Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	V_{GS} = - 20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	1		3	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance	V_{GS} = 10 V, I_D = 26 A V_{CS} = 4.5 V, I_D = 21A		0.014	0.015 0.025	Ω
$I_{D(ON)}$	ON-State Drain Current	V_{GS} = 10 V	60			A

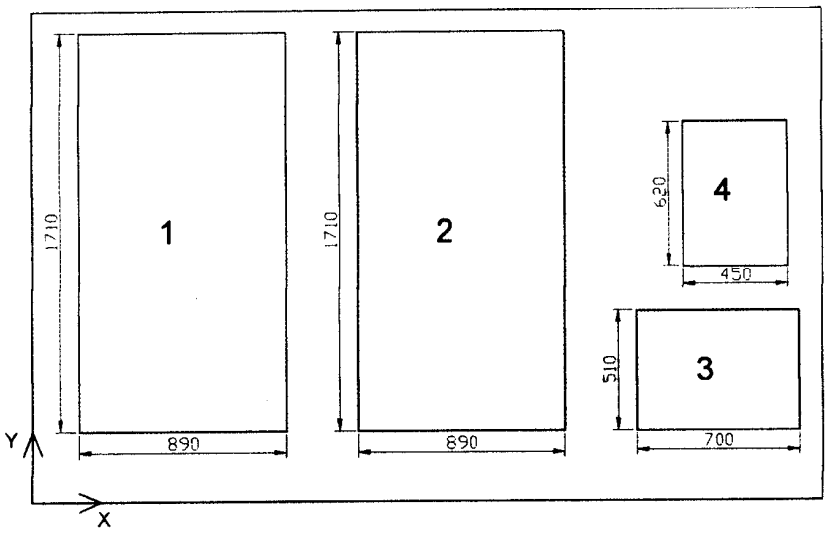
Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 26 A		32		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz			1500	pF
C_{oss}	Output Capacitance				700	pF
C_{rSS}	Reverse Transfer Capacitance				300	pF
SWITCHING CHARACTERISTICS (Note)						
$t_{D(ON)}$	Turn-ON Delay Time	V_{DD} = 15 V, I_D = 52 A, V_{GS} = 10 V, R_{GEN} = 24 Ω			60	nS
t_r	Turn-ON Rise Time				200	nS
$t_{D(OFF)}$	Turn-OFF Delay Time				50	nS
t_f	Turn-OFF Fall Time				120	nS

SOURCE—DRAIN DIODE CHARACTERISTICS				
I_S	Maximum Continuous Drain-Source Diode Forward Current		60	A
V_{SD} (Note)	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 26 A	1.35	V
THERMAL CHARACTERISTICS				
$R_{\theta JC}$	Thermal Resistance, Junction to Case		2.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		62.5	°C/W

Note: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0 %

Pad Location



Chip size 3.00 mm x 2.07 mm

Pad	Pad Name	Coordinates, μm	
		X	Y
1	Source	179	177
2	Source	1150	177
3	Source	2122	177
4	Gate	2400	722

Thickness of the metallization (Al + Si) – (2.5 μm ± 0.3 μm)
Metal of the back side Ti/Ni/Ag
Thickness of the back side metallization: Ti/Ni/Ag – 0.15 μm/ 0.25 μm/ 1.2 μm ± 10%
Thickness of the plate (350 ± 30) μm
Passivation SiON
Thickness of the passivation (0.7 ± 0.1) μm